

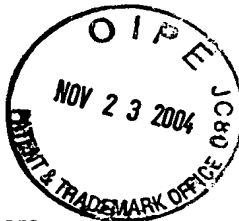
IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Philip J. Kuekes, et al.

Application No.: 09/699,080

Filing Date: March 29, 1999

Title: Molecular Wire Transistors



Confirmation No.: 5511

Examiner: D.A. Wille

Group Art Unit: 2814

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

- ☒ under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)
- ☐ under 37 CFR 1.97 (c) together with either a:
☐ Statement under 37 CFR 1.97(e), or
☐ a \$180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)
- ☐ under 37 CFR 1.97 (d) together with a:
☐ Statement under 37 CFR 1.97(e)(1) or (2), and
☐ a \$180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of \$0.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

☒ Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

☐ A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

- ☐ I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: _____
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Respectfully submitted,

Philip J. Kuekes, et al.

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Date: Nov. 22, 2004

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PATENT APPLICATION

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FORM PTO-1449	ATTY. DOCKET NO. PD-10981967-2	SERIAL NO. 09/699,080
APPLICANT Philip J. Kuekes, et al.		
FILING DATE 3/29/99	GROUP	

REFERENCE DESIGNATION OF U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
	5665618	09/1997	Meyer, et al	438/172	
	5646418	07/1997	Frazier et al.	257/4	

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLAS	TRANSLATION	
						YES	NO

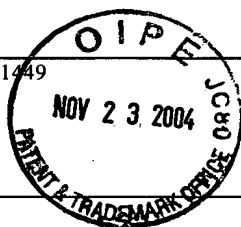
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	L. Guo et al., "Nanoscale silicon field effect transistors fabricated using imprint lithography," <u>Applied Physics Letters</u> , Vol. 71, pp. 1881-1883 (29 September 1997)
	L. Guo et al., "A Single-Electron Transistor Memory Operating at Room Temperature," <u>Science</u> , Vol. 2756, pp. 649-651 (31, January 1997)
	S.J. Tans et al., "Room-temperature transistor based on a single carbon nanotube," <u>Nature</u> , Vol. 393, pp. 49-52 (7 May 1998)
	K.K. Likharev, "Correlated discrete transfer of single electrons in ultrasmall tunnel junctions", <u>IBM Journal of Research and development</u> , Vol. 32, pp. 144-158 (January 1998)

EXAMINER

DATE CONSIDERED

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GROUP

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLAS	TRANSLATION	
						YES	NO

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	Heath, "A defect-Tolerant Computer Architecture: Opportunities for Nanotechnology", <u>Science</u> , Vol. 280, pp. 1716-1721 (June 12, 1998)

EXAMINER

DATE CONSIDERED